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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,597	12/18/2001	Gilbert Yoh	10011042-1	2843

7590 11/01/2005

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EXAMINER	
WARE, CICELY Q	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/046,597	YOH ET AL.	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11,14-18 and 21-25* is/are rejected.

7)☐ Claim(s) *12,13,19,20,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Keeth et al. (US Patent Application 2002/0118563).

(1) With regard to claim 21, Keeth et al. discloses in (Fig. 1) a system comprising: a register having a clock input and a data input (13); a clock receiver (11) for receiving a clock signal; at least one clock buffer for driving the clock signal to the register (Pg. 1, col. 2, lines 1-6, 57-65); a data receiver (15) for receiving a data signal; and at least one data delay device; wherein the at least one data delay device is configured to substantially match the delay of the clock signal from the clock receiver to the clock

input of the register with the delay of the data signal from the data receiver to the data input of the register (Pg. 1, col. 1, lines 10-38).

(2) With regard to claim 22, claim 22 inherits all the limitations of claim 21. Keeth et al. further discloses wherein the at least one data delay device is configured to mimic the delay of the at least one clock buffer (Pg. 1, col. 1, lines 10-38).

(3) With regard to claim 23, claim 23 inherits all the limitations of claim 21. Keeth et al. further discloses wherein the number of the at least one data delay device is equal to the number of the at least one clock buffer (Pg. 1, col. 1, lines 10-38, col. 2, lines 1-6).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 9, 10, 15, 16, 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US Patent 6,240,524) in view of Pasqualini (US Patent Application 2002/0023253).

(1) With regard to claim 8, Suzuki discloses formulating at least one miniaturized clock buffer located with in said receive logic, wherein said at least one miniaturized clock buffer is a scaled version of said clock buffer, said miniaturized version of said clock buffer having a scaling factor of K, said scaling factor representing a number of

said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer (col. 5, lines 53-67, col. 6, lines 1-25, 34-44, col. 12, lines 27-38); and minimizing negative variations experienced by said clock buffer (col. 1, lines 50-55, col. 3, lines 4-7).

However Suzuki does not disclose minimizing setup and hold times of said receive logic.

However Pasqualini discloses minimizing setup and hold times of said receive logic (Pg. 1, lines 37-67 – col. 2, lines 1-5, 17-21).

Therefore it would have been obvious to one of ordinary skill in the art to modify Suzuki in view of Pasqualini to incorporate formulating at least one miniaturized clock buffer located with in said receive logic, wherein said at least one miniaturized clock buffer is a scaled version of said clock buffer, said miniaturized version of said clock buffer having a scaling factor of K, said scaling factor representing a number of said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer; and minimizing negative variations experienced by said clock buffer in order to allow for complete voltage excursions between VCC and ground and keep the data delays from varying with the data rate (Pasqualini, Pg. 4, lines 40-46).

(2) With regard to claim 9, claim 9 inherits all the limitations of claim 8. Suzuki further discloses wherein said receive logic is situated on an application specific integrated circuit (col. 1, lines 5-17).

(3) With regard to claim 10, claim 10 inherits all the limitations of claim 8. Pasqualini further discloses wherein said negative variations are selected from the

group consisting of process, voltage and temperature (abstract, Pg. 4, col. 2, lines 10-22).

(4) With regard to claim 15, see rejection of claim 8.

(5) With regard to claim 16; claim 16 inherits all the limitations of claim 15. See rejection of claim 9.

(6) With regard to claim 17, claim 17 inherits all the limitations of claim 15. See rejection of claim 10.

6. Claims 11, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US Patent 6,240,524) in view of Pasqualini (US Patent Application 2002/0023253) as applied to claims 8 and 15, in further view of Keeth et al. (US Patent Application 2002/0118563).

(1) With regard to claim 11, claim 11 inherits all the limitations of claim 8. Pasqualini in combination with Suzuki disclose all the limitations of claim 8. However Pasqualini in combination with Suzuki do not disclose wherein said clock buffer is capable of driving a received clock signal to a register located within said receive logic.

However Keeth et al. discloses wherein said clock buffer is capable of driving a received clock signal to a register located within said receive logic (Pg. 1, col. 2, lines 1-6).

Therefore it would have been obvious to one of ordinary skill in the art to modify the inventions of Pasqualini in combination with Suzuki in view of Keeth et al. to incorporate wherein said clock buffer is capable of driving a received clock signal to a

register located within said receive logic in order to track instantaneous changes in delay of the clock or data circuits (Keeth et al., Pg. 1, col. 1, lines 50-53).

(2) With regard to claim 14, claim 14 inherits all the limitations of claim 8. Keeth et al. further discloses wherein said clock buffer provides an amount of delay that slows progression of said clock signal in a path to a register located within said receive logic (Pg. 1, col. 1, lines 10-38).

(3) With regard to claim 18, claim 18 inherits all the limitations of claim 15. See rejection of claim 11.

7. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth et al. (US Patent Application 2002/0118563) as applied to claim 21, in view of Pasqualini (US Patent Application 2002/0023253).

(1) With regard to claim 24, claim 24 inherits all the limitations of claim 23. However Keeth et al. does not disclose wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power and load.

However Pasqualini discloses wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power and load (Pg. 4, col. 2, lines 57-61).

Therefore it would have been obvious to one of ordinary skill in the art to modify wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power and load in order to provide the total

data delay required to operate an IC under a zero hold time constraint at its clock/data pins (Pasqualini, Pg. 4, col. 1, lines 48-50).

(2) With regard to claim 25, claim 25 inherits all the limitations of claim 21. Pasqualini further discloses wherein the delay of the at least one clock buffer is subject to variations, and the at least one data delay device is configured to duplicate the variations (Pg. 2, col. 2, lines 43-64).

Allowable Subject Matter

8. Claims 12, 13, 19, 20, 26 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: The instant application discloses a system for matching data and clock signal delays. Prior art references show similar methods but fail to teach: **"a setup time of said receive logic is represented by the equation: T.sub.setup=T.sub.reg-setup+1.1.times.(-T.sub.clk-dly)-T.sub.clk-rte(min) wherein, T.sub.reg-setup is a setup time for said register, T.sub.clk-dly is a delay contributed by said clock buffer, and T.sub.clk-rte(min) is a minimum delay contributed by propagation of said clock signal to said register"**, as in claim 12, 19, 26; and **"a hold time of said receive logic is represented by the equation: T.sub.hold=T.sub.reg-hold+1.1.times.(T.sub.c- lk-dly)+T.sub.clk-rte(max) wherein, T.sub.reg-hold is a hold time for said register, T.sub.clk-dly) is a delay contributed by said clock buffer, and T.sub.clk-rte(max)**

is a maximum delay contributed by propagation of said clock signal to said register", as in claim 13, 20, 27.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
October 31, 2005

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600